AMENDMENTS TO THE ABSTRACT OF DISCLOSURE

Please replace the Abstract of the Disclosure with the following amended Abstract of the Disclosure:

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device, a first memory cell having a first gate electrode, a first diffusion layer and a second diffusion layer, the first and second diffusion layers arranged in a semiconductor substrate to be adjacent to the first gate electrode; a first contact layer connected to the first diffusion layer of the first memory cell; a second contact layer connected to the first contact layer; a first bit line connected to the second contact layer and arranged above the first gate electrode of the first memory cell; a second memory cell having a second gate electrode, a third diffusion layer and a fourth diffusion layer, the third and fourth diffusion layers arranged in a semiconductor substrate to be adjacent to the second gate electrode, the second gate electrode of the second memory cell electrically connected to the first gate electrode of the first memory cell, the first and second memory cells arranged in a direction perpendicular to the first bit line; a second bit line connected to the third diffusion layer, arranged above the second gate electrode of the second memory cell, and arranged parallel to the first bit line; and a conductive layer commonly connected to the second diffusion layer of the first memory cell and the fourth diffusion layer of the second memory cell, a height of the conductive layer substantially being coplanar with a height of the first contact layer ~~A semiconductor memory device having a gate electrode and a diffusion layer, comprising a plurality of memory cells each of which including the gate electrode and the diffusion layers; a first contact layer connected to one of the diffusion layer of the memory cell; a second contact layer connected to the first contact layer; a bit line connected to the second contact layer; and a conductive layer connected to at least two of the diffusion layers~~

~~that are other than the diffusion layer connected to the first contact layer, at least two of the diffusion layers being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being the same as a height of the first contact layer~~.